# CH132 Datasheet

V2.2

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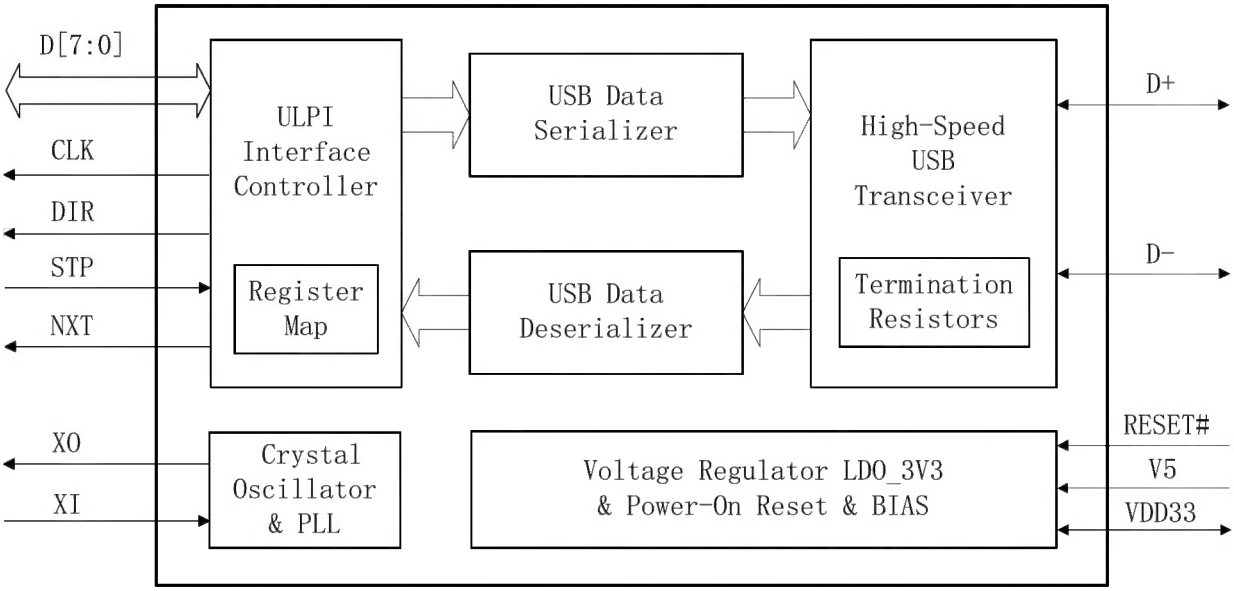
## Overview

CH132 is a high-speed USB transceiver chip (USB PHY, High Speed Transceiver) with ULPI interface, compatible with USB 2.0 protocol specification and UTMI+ Low Pin Interface (ULPI) 1.1 protocol specification. It supports USB2.0 high-speed 480Mbps, full-speed 12Mbps and low-speed 1.5Mbps data transmission and reception, and can be used to extend the USB host port or device port for MCU or FPGA with ULPI interface.



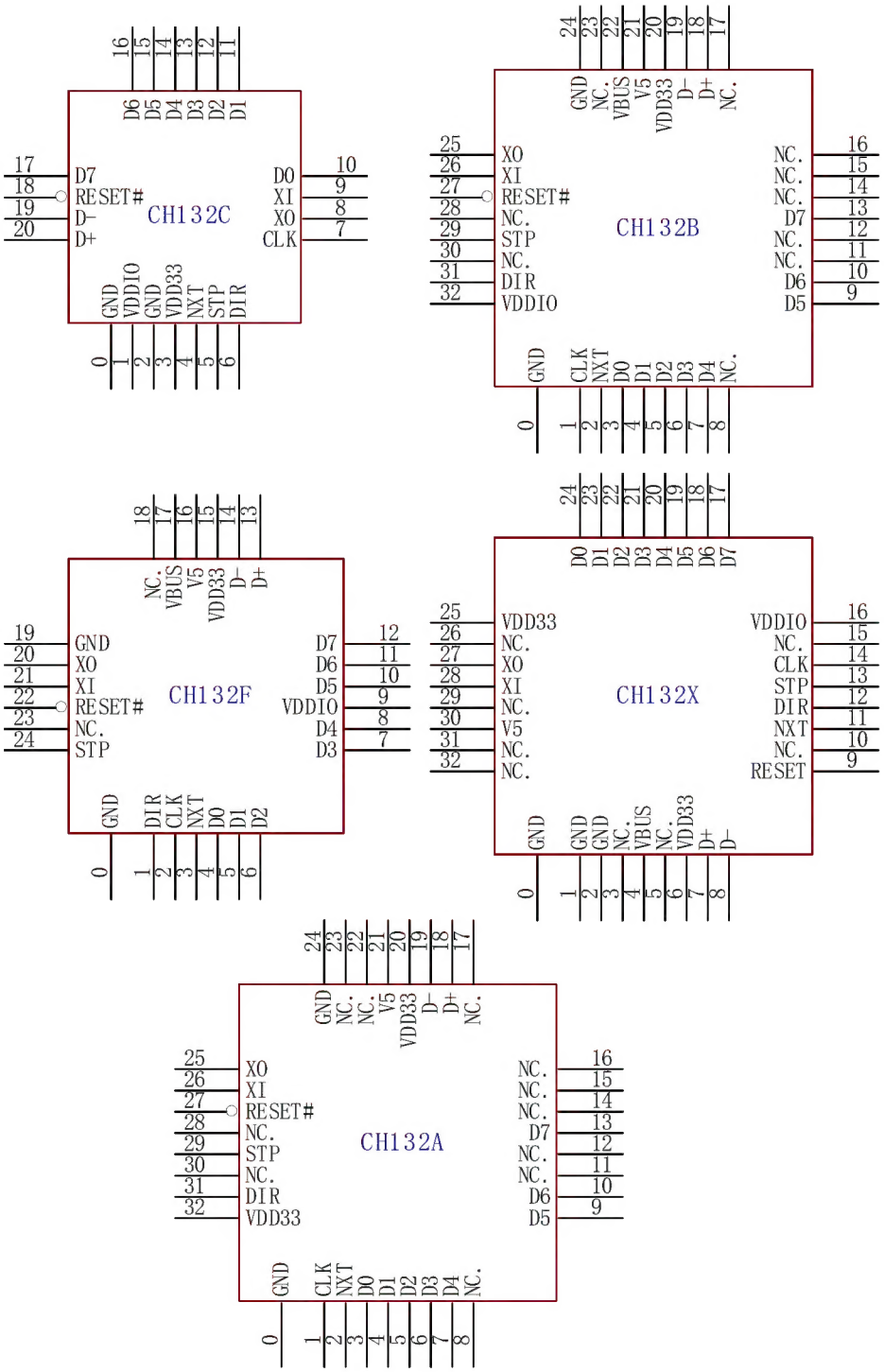

## Features

- Compatible with USB Specification Rev. 2.0.
- Compatible with UTMI+ Low Pin Interface (ULPI) Rev 1.1.
- 12-pin ULPI interface, 1.8V~3.3V I/O level, 60MHz clock.
- Support USB host and USB device.
- Support USB High-speed, Full-speed and Low-speed.
- Support 3-pin or 6-pin Full-Speed or Low-Speed serial mode.
- Support D+ and D- signal line switching modes
- Built-in 3.3V low dropout linear regulator, support 3.3V or 5V supply input.
- Built-in power-on reset circuit, built-in clock oscillator and PLL.
- Built-in impedance matching resistor, built-in oscillation capacitor, with lower BOM cost.
- Support ULPI input clock and output clock modes
- USB pin with 6KV enhanced ESD performance.
- Industrial-grade temperature range: -40 to 85°C.
- Available in QFN24 and QFN32 packages.

# Chapter 1 Pin Information

## 1.1 Pinouts

Figure 1-1 Pinouts




*Note: Pin 0# is the EPAD of QFN package.*

## 1.2 Packages

Table 1-1 Package description

| Package Form | Body Size | | Pin Pitch | | Package Description | Order Model |
|---|---|---|---|---|---|---|
| QFN20C_2x2 | 2*2mm | | 0.32mm | 12.6mil | Quad Flat No-Lead Package | CH132C |
| QFN24_4x4 | 4*4mm | | 0.5mm | 19.7mil | Quad Flat No-Lead Package | CH132F |
| QFN32_5x5 | 5*5mm | | 0.5mm | 19.7mil | Quad Flat No-Lead Package | CH132B |
| QFN32_5x5 | 5*5mm | | 0.5mm | 19.7mil | Quad Flat No-Lead Package | CH132A |
| QFN32_5x5 | 5*5mm | | 0.5mm | 19.7mil | Quad Flat No-Lead Package | CH132X |

*Note:*
*The CH132B is based on the CH132A upgrades with the addition of the VDDIO pin and is forward compatible with the CH132A pin.*
*CH132C/F/B/X is available for new designs, and it is recommended that the smaller CH132C is preferred.*

## 1.3 Pin Definitions

Table 1-2 CH132 pin definitions

| Pin No. | | | | | Pin name | Type | Function Description |
|---|---|---|---|---|---|---|---|
| 132C | 132F | 132H 132A | 132B | 132X | | | |
| 20 | 13 | 18 | 18 | 7 | D+ | USB | USB2.0 high-speed differential signal lines DP |
| 19 | 14 | 19 | 19 | 8 | D- | USB | USB2.0 high-speed differential signal lines DM |
| - | - | 1 | - | - | CLK | O | ULPI 60MHz clock signal output |
| 7 | 2 | - | 1 | 14 | CLK | I/O | ULPI 60MHz clock signal output or 60MHz clock signal input |
| 4 | 3 | 2 | 2 | 11 | NXT | O | ULPI Next signal output |
| 6 | 1 | 31 | 31 | 12 | DIR | O | ULPI Direction signal output |
| 5 | 24 | 29 | 29 | 13 | STP | I | ULPI Stop signal input, built-in controlled pull-up current |
| 10 | 4 | 3 | 3 | 24 | D0 | I/O | ULPI bidirectional DATA0, built-in weak pull-down resistor |
| 11 | 5 | 4 | 4 | 23 | D1 | I/O | ULPI bidirectional DATA1, built-in weak pull-down resistor |
| 12 | 6 | 5 | 5 | 22 | D2 | I/O | ULPI bidirectional DATA2, built-in weak pull-down resistor |
| 13 | 7 | 6 | 6 | 21 | D3 | I/O | ULPI bidirectional DATA3, built-in weak pull-down resistor |
| 14 | 8 | 7 | 7 | 20 | D4 | I/O | ULPI bidirectional DATA4, built-in weak pull-down resistor |
| 15 | 10 | 9 | 9 | 19 | D5 | I/O | ULPI bidirectional DATA5, built-in weak pull-down resistor |
| 16 | 11 | 10 | 10 | 18 | D6 | I/O | ULPI bidirectional DATA6, built-in weak pull-down resistor |
| 17 | 12 | 13 | 13 | 17 | D7 | I/O | ULPI bidirectional DATA7, built-in weak pull-down resistor |
| - | - | 26 | - | - | XI | IL | Crystal input, external 12MHz crystal one end, or external |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | | | | | clock input |
| 9 | 21 | - | 26 | 27 | XI | IL | Crystal input, external 12MHz crystal one end, or external clock input, or shorting GND selects ULPI clock mode from CLK pin. |
| 8 | 20 | 25 | 25 | 28 | XO | OL | Inverted output of crystal oscillator, need to connect the other end of the external 12MHz crystal |
| 18 | 22 | 27 | 27 | - | RESET # | I | Reset signal input, active low, built-in pull-up resistor |
| - | - | - | - | 9 | RESET | I | Reset signal input, active high, built-in pull-down resistor |
| - | 17 | - | 22 | 4 | VBUS | I | VBUS detect input, active high, built-in pull-up resistor. Some models or lot numbers do not support VBUS, it is recommended to suspend or short VDD33 |
| - | 16 | 21 | 21 | 30 | V5 | P | 5V or 3.3V power input, external 1uF~4.7uF decoupling capacitor |
| - | 15 | 20 | 20 | 6 | VDD33 | P | LDO output and 3.3V power input, external 1uF~4.7uF decoupling capacitor |
| 3 | - | 32 | - | 25 | VDD33 | P | 3.3V power input |
| 1 | 9 | - | 32 | 16 | VDDIO | P | ULPI interface I/O signal supply voltage, support 1.8V, 2.5V, 3.3V voltage, external 0.1uF decoupling capacitor |
| 2 | 19 | 24 | 24 | 1, 2 | GND | P | Common ground, optional but GND connection recommended |
| 0 | 0 | 0 | 0 | 0 | GND | P | Common ground (QFN EPAD), necessary connection |
| - | 18, 23 | 8, 11, 12, 14, 15, 16, 17, 22, 23, 28, 30 | 8, 11, 12, 14, 15, 16, 17, 22, 23, 28, 30 | 3, 4, 5, 10, 15, 26, 29, 31, 32 | NC. | - | Empty or reserved pins, connection prohibited |

Pin type:

(1) I: 3.3V signal input for CH132A, VDDIO voltage signal input for CH132C/F/B/X.
(2) O: 3.3V signal output for CH132A, VDDIO voltage signal output for CH132C/F/B/X.
(3) IL: Signal input for rated 1.2V voltage, supports signal input for 1.2V to 1.4V voltage.
(4) OL: Signal output for rated 1.2V voltage.
(5) P: Power or ground
(6) USB: USB signal

# Chapter 2 Basic Functions

## 2.1 Clock and Reset

### 2.1.1 Clock Source

The CH132 requires a 12 MHz clock source, either by inputting the clock from pin XI and leaving XO suspended, or by connecting an external 12MHz crystal to pins XI and XO to generate the clock source via an internal oscillator. The CH132 then generates the multiple clocks required by the chip via PLL:

- 1.5MHz clock for USB low-speed data transfer
- 12MHz clock for USB full-speed data transfer
- 480MHz clock for USB high-speed data transfer
- 60MHz clock for ULPI controller
- Other clocks required for internal data processing

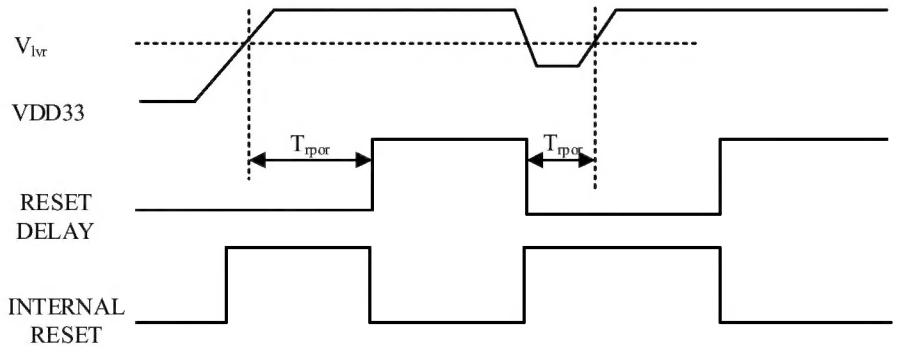
By default, the ULPI clock mode is output, and a 60MHz clock is output from the CLK pin to the ULPI LINK.

CH132C/F/B/X also supports input ULPI clock mode. During power-on reset, if CH132 detects that the XI pin is shorted to GND, the CLK pin is the clock input, and the ULPI LINK provides a 60MHz clock, and CH132 generates required for each clock.

### 2.1.2 Power-on Reset

The CH132 has a built-in power-on reset module, which generally does not require an external reset signal. When the power supply is powered on, the chip's internal POR power-on reset module will generate a power-on reset timing and delay Trpor to wait for the power supply to stabilize. During operation, when the power supply voltage falls below $V_{lvr}$, the chip's internal low voltage reset (LVR) module generates a low voltage reset until the voltage rises back up and delays for the power supply to stabilize. Figure 2-1 shows the power-on reset process as well as the low voltage reset process.

Figure 2-1 Power-on reset




### 2.1.3 External Reset

The external reset input pin RESET# contains a pull-up resistor of about 24KΩ, and if the chip needs to be reset externally, the pin can be driven low (open-drain drive is recommended) with a low pulse width of at least Twreset. It is recommended not to attach an external pull-up resistor.

The CH132X's external reset input pin, RESET, has a built-in pull-down resistor, and driving this pin high will reset the chip.

## 2.2 Power Supply

The CH132 has a built-in low dropout linear regulator LDO. 3.3V supply by default, 5V supply is also supported.

For the 3.3V power supply system, the 3.3V power supply is input to the VDD33 pin and the V5 pin at the same time for internal analog circuits.
For a 5V power supply system, the 5V power supply is input to the V5 pin, and the internal LDO generates a 3.3V power supply at the VDD33 pin for internal analog circuitry. The CH132C does not have a V5 pin and does not support a 5V supply.
In both ways, external decoupling capacitors are required on the VDD33 and V5 pins, and VDD33 is recommended to be 0.1uF in parallel with 10uF or 4.7uF.
Avoid feeding the 5V power from VBUS directly into V5 pin. It is recommended that an overvoltage protection circuit be added between VBUS pin and V5 pin.
For CH132C/F/B/X, the VDDIO pin is used for I/O circuit power supply and supports 1.8V, 2.5V, and 3.3V voltages. For CH132A, the VDD33 pin is also used for I/O circuit power supply and supports 3.3V only.

## 2.3 USB Transceiver

The CH132 USB transceiver takes on USB high-speed, full-speed and low-speed data transceiver tasks. Transceiver includes the differential driver circuitry necessary for USB high-speed, full-speed and low-speed data transmission, the differential and single ended receivers for USB high-speed, full-speed and low-speed data reception, the circuitry to detect high-speed bus activity and the circuitry to detect high-speed bus disconnection. The USB port has a variety of built-in matching resistors, including impedance matching resistors, device pull-up resistors, host pull-down resistors, etc.
A detailed relationship between the registers and the USB port mode can be found in Table 2-1 below.

Table 2-1 Register settings and port mode relationships

| USB port mode | Register settings | | | | |
|---|---|---|---|---|---|
| | XCVR SELECT[1:0] | TERM SELECT | OP MODE[1:0] | DP_ PULLDOWN | DM_ PULLDOWN |
| 3-state drivers | xxb | x | 01b | x | x |
| Host Chirp | 00b | 0 | 10b | 1 | 1 |
| Host High-speed | 00b | 0 | 00b | 1 | 1 |
| Host Full-speed | x1b | 1 | 00b | 1 | 1 |
| Host High-speed or Full-speed suspend | 01b | 1 | 00b | 1 | 1 |
| Host High-speed or Full-speed resume | 01b | 1 | 10b | 1 | 1 |
| Host Low-speed | 10b | 1 | 00b | 1 | 1 |
| Host Low-speed suspend | 10b | 1 | 00b | 1 | 1 |
| Host Low-speed resume | 10b | 1 | 10b | 1 | 1 |
| Host Test J or Test K | 00b | 0 | 10b | 1 | 1 |
| Peripheral Chirp | 00b | 1 | 10b | 0 | 0 |
| Peripheral High-speed | 00b | 0 | 00b | 0 | 0 |
| Peripheral Full-speed | 01b | 1 | 00b | 0 | 0 |
| Peripheral High-speed or Full-speed suspend | 01b | 1 | 00b | 0 | 0 |
| Peripheral High-speed or Full-speed resume | 01b | 1 | 10b | 0 | 0 |
| Peripheral Test J or Test K | 00b | 0 | 10b | 0 | 0 |

## 2.4 ULPI Controller

The CH132 provides a 12 Pin interface compatible with the ULPI (UTMI+ Low Pin Interface) 1.1 protocol. This interface should be connected to the ULPI interface of the ULPI LINK, which has a USB controller at the other end.

This ULPI interface controller has the following functions:

- ULPI protocol compatible interface and register settings
- Allow functional control via USB host or peripheral devices
- Parse data transmitted or received by USB
- Prioritize USB data transmitting and receiving, interrupts and register operations
- 3-pin serial mode
- 6-pin serial mode

## 2.5 ULPI RX CMD Data

Table 2-2 RXCMD data bit format

<table>
<tr><th>Bit</th><th>Name</th><th>Default</th><th colspan="4">Description</th></tr>
<tr><td>[1:0]</td><td>LineState</td><td>00b</td><td colspan="4">Corresponds to UTMI+ LineState two signals:<br>LineState[0] corresponds to receiving single-ended data from DP,<br>LineState[1] corresponds to receiving single-ended data from DM.</td></tr>
<tr><td>[3:2]</td><td>Reserved</td><td>00b</td><td colspan="4">Reserved, always 00.</td></tr>
<tr><td rowspan="6">[5:4]</td><td rowspan="6">RxEvent</td><td rowspan="6">00b</td><td colspan="4">UTMI event signal encoding:</td></tr>
<tr><td>Value</td><td>RxActive</td><td>RxError</td><td>HostDisconnect</td></tr>
<tr><td>00</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>01</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>11</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>10</td><td>X</td><td>X</td><td>1</td></tr>
<tr><td>6</td><td>Reserved</td><td>0b</td><td colspan="4">Reserved, always 0.</td></tr>
<tr><td>7</td><td>Reserved</td><td>0b</td><td colspan="4">Reserved, data should be ignored.</td></tr>
</table>

## 2.6 3-pin and 6-pin Serial Mode

The CH132 provides either 3-pin or 6-pin serial modes. Select the serial mode of the 3-wire or 6-wire interface as needed to transfer full-speed or low-speed USB packets. 3-wire serial mode interface mapping is shown in Table 2-3, and 6-wire serial mode interface mapping is shown in Table 2-4.

Entering or exiting the 3-pin or 6-pin serial mode can be described in the R8_INTF_CTRL register regarding the 3PIN_FSLS_SERIAL or 6PIN_FSLS _SERIAL bit is described.

Table 2-3 Signal mapping for 3-pin serial

| Signal | Maps to | Direction | Description |
|---|---|---|---|
| TX_ENABLE | DATA0 | I | Mode selection, transmit enable. Active high.<br>0: Receive data;<br>1: Transmit data. |
| DAT | DATA1 | I/O | When TX_ENABLE = 1, transmit differential data on DP and DM.<br>When TX_ENABLE = 0, receive differential data from DP and DM. |
| SE0 | DATA2 | I/O | When TX_ENABLE = 1, transmit single-ended zero |

| Signal | Maps to | Direction | Description |
|---|---|---|---|
| | | | on DP and DM.<br>When TX_ENABLE = 0, receive single-ended zero from DP and DM. |
| Reserved | DATA3 | O, PD | Reserved, CH132 pin output data should be ignored. |
| Reserved[7:4] | DATA[7:4] | O, PD | Reserved, CH132 pin provides pull-down resistor or output low. |

Table 2-4 Signal mapping for 6-pin serial

| Signal | Maps to | Direction | Description |
|---|---|---|---|
| TX_ENABLE | DATA0 | I | Transmit enable. Active high. |
| TX_DAT | DATA1 | I | Transmit differential data on DP and DM |
| TX_SE0 | DATA2 | I | Transmit single-ended zero on DP and DM |
| Reserved | DATA3 | O, PD | Reserved, CH132 pin output data should be ignored. |
| RX_DP | DATA4 | O | Receive single-ended data from DP |
| RX_DM | DATA5 | O | Receive single-ended data from DM |
| RX_RCV | DATA6 | O | Receive differential data from DP and DM |
| Reserved | DATA7 | O, PD | Reserved, CH132 pin provides pull-down resistor or output low. |

# Chapter 3 ULPI Registers

## 3.1 Register Description

The following abbreviations may be used in this datasheet when describing registers:

| Register bit attributes | Description |
|---|---|
| RO | Read-only. Data is generated and changed by hardware. |
| WO | Write-only (This bit cannot be read, and the read value is uncertain) |
| RW | Readable and writable. |

Description of registers related to ULPI interface operation of CH132 series chips. The default is based on CH132B and CH132C/F/X. For other models such as CH132A or CH132H, please note if there are any differences.

Table 3-1 CH132 ULPI registers

| Name | Address (6 bit) | | | | Description | Reset Value |
|---|---|---|---|---|---|---|
| | Read | Write | Set | Clear | | |
| R8_VENDOR_ID_L | 0x00 | - | - | - | Low byte of manufacturer ID register | 0x86 [Note 10] |
| R8_VENDOR_ID_H | 0x01 | - | - | - | High byte of manufacturer ID register | 0x1A [Note 11] |
| R8_PRODUCT_ID_L | 0x02 | - | - | - | Low byte of manufacturer ID register | 0x32 [Note 12] |
| R8_PRODUCT_ID_H | 0x03 | - | - | - | High byte of manufacturer ID register | 0x01 [Note 13] |
| R8_FUNC_CTRL | 0x04–0x06 | 0x04 | 0x05 | 0x06 | ULPI function control register | 0x41 [Note 1] |
| R8_INTF_CTRL | 0x07–0x09 | 0x07 | 0x08 | 0x09 | ULPI interface control register | 0x00 |
| R8_OTG_CTRL | 0x0A–0x0C | 0x0A | 0x0B | 0x0C | OTG control register | 0x06 [Note 2] |
| R8_USB_INTR_EN_R | 0x0D–0x0F | 0x0D | 0x0E | 0x0F | USB rising interrupt enable register | 0x01 [Note 2] |
| R8_USB_INTR_EN_F | 0x10–0x12 | 0x10 | 0x11 | 0x12 | USB falling interrupt enable register | 0x01 [Note 2] |
| R8_USB_INTR_STAT | 0x13 | - | - | - | USB interrupt status register | 0x00 |
| R8_USB_INTR_L | 0x14 | - | - | - | USB interrupt latch register | 0x00 |
| R8_SCRATCH | 0x16–0x18 | 0x16 | 0x17 | 0x18 | Scratch register | 0x00 |
| R8_USB_IO_SWAP | 0x39–0x3B | 0x39 | 0x3A | 0x3B | | 0x00 [Note 14] |
| | Other | | | | Reserved | 0x00 |

(1) R: Read, readable register. Read-only if there is no corresponding W/S/C.
(2) W: Write, the register is written, the new data will overwrite the original data of this register directly during the operation.
(3) S: Set, register by position 1, the new data will be written with the original data of this register by bit or operation.
(4) C: Clear, the register is cleared by bit, the new data will be written with the original data of this register after bit and operation.

*Note 10, Note 11, Note 12, Note 13: 0x00 for CH132A.*
*Note 14: This register is not supported for CH132A.*

Recommendation:

Set the target parameters to the R8_FUNC_CTRL and R8_OTG_CTRL registers after each power-up or reset, regardless of the original values.
No need to manipulate and use each register of R8_USB_INTR_*, which can be implemented with RxEvent/LineState status in RXCMD.

ULPI function control register (R8_FUNC_CTRL, Address R = 04h/05h/06h, W = 04h, S = 05h, C = 06h)

| Bit | Symbol | Access | Description | Reset Value |
|---|---|---|---|---|
| 7 | Reserved | RO | Reserved | 0 |
| 6 | SUSPEND | RW | **Suspend:**<br>Enter low-power mode. Active low. The ULPI linker can exit low power mode through STP. This bit is automatically set to 1 when the CH132 exits low power mode.<br>**0**: Low power mode.<br>**1**: Normal. | 1 |
| 5 | RESET | RW | **Internal Reset:**<br>Active high. This does not reset the ULPI interface or the ULPI register.<br>When the reset is completed, the CH132 will desert DIR and automatically clear this bit.<br>**0**: Normal;<br>**1**: Enable reset. | 0 |
| [4:3] | OP MODE | RW | **Operation Mode:**<br>Selects the required bit-encoding style during transfer<br>**00**: Normal;<br>**01**: Not drive;<br>**10**: Disable bit-stuffing and NRZI encoding;<br>**11**: Reserved. | 00b |
| 2 | TERM SELECT | RW | **Termination selection:**<br>Controls the pull-up/pull-down resistor and high-speed terminations, depending on XCVR SELECT, OP MODE, DP_PULLDOWN and DM_PULLDOWN.<br>As shown in Table 2-1 | 0 |
| [1:0] | XCVR SELECT | RW | **Transceiver selection:**<br>**00**: Enable the high-speed transceiver<br>**01**: Enable the full-speed transceiver<br>**10**: Enable the low-speed transceiver<br>**11**: Enable the full-speed transceiver for low-speed packets (full-speed preamble is automatically prefixed) | 01b |

ULPI interface control register (R8_INTF_CTRL, Address R = 07h/08h/09h, W = 07h, S = 08h, C = 09h)

| Bit | Symbol | Access | Description | Reset Value |
|---|---|---|---|---|
| 7 | INTF_PROT_DIS | RW | **Disable interface protect:**<br>The ULPI interface protection circuitry built into the control chip when the ULPI linker is not output to STP and DATA[7:0]<br>**0**: Enable ULPI interface protection circuit, enable STP weak pull-ups;<br>**1**: Disable ULPI interface protection circuit, disable STP weak pull-ups. | 0 |

| | | | | |
|---|---|---|---|---|
| [6:2] | Reserved | RO | Reserved | 00000b |
| 1 | 3PIN_FSLS_SERIAL | RW | **3-Pin full-speed and low-speed serial mode:**<br>Changes the ULPI interface into a 3-pin serial interface. The CH132 automatically clears this bit when the mode is exited.<br>**0**: Disables 3-pin serial mode, full-speed low-speed packet transfer via ULPI parallel port;<br>**1**: Enables 3-pin serial mode, full-speed low-speed packet transmission over 3-pin interface | 0 |
| 0 | 6PIN_FSLS_SERIAL | RW | **6-Pin full-speed and low-speed serial mode:**<br>Changes the ULPI interface into a 3-pin serial interface. The CH132 will automatically clear this bit when the mode is exited.<br>**0**: Disables 6-pin serial mode, full-speed low-speed packet transfer via ULPI parallel port;<br>**1**: Enables 6-pin serial mode, full-speed low-speed packet transmission over 6-pin interface | 0 |

OTG control register (R8_OTG_CTRL, Address R = 0Ah/0Bh/0Ch, W = 0Ah, S = 0Bh, C = 0Ch)

| Bit | Symbol | Access | Description | Reset Value |
|---|---|---|---|---|
| [7:3] | Reserved | RO | Reserved | 00000b |
| 2 | DM_PULLDOWN | RW | **DM pull-down enable:**<br>**0:** DM pull-down resistor disabled<br>**1:** DM pull-down resistor enabled | 1 |
| 1 | DP_PULLDOWN | RW | **DP pull-down enable:**<br>**0:** DP pull-down resistor disabled<br>**1:** DP pull-down resistor enabled | 1 |
| 0 | Reserved | RO | Reserved | 0 |

USB rising interrupt enable register (R8_USB_INTR_EN_R, Address R = 0Dh/0Eh/0Fh, W = 0Dh, S = 0Eh, C = 0Fh)

| Bit | Symbol | Access | Description | Reset Value |
|---|---|---|---|---|
| [7:1] | Reserved | RO | Reserved | 0000000b |
| 0 | HOST_DISCON_R | RW | **Host disconnect rise:**<br>Enable Interrupts for logic 0 to logic 1 transitions on HOST_DISCON | 1 |

USB falling interrupt enable register (R8_USB_INTR_EN_F, Address R = 10h/11h/12h, W = 10h, S = 11h, C = 12h)

| Bit | Symbol | Access | Description | Reset Value |
|---|---|---|---|---|
| [7:1] | Reserved | RO | Reserved | 0000000b |
| 0 | HOST_DISCON_F | RW | **Host disconnect rise:**<br>Enable Interrupts for logic 1 to logic 0 transitions on HOST_DISCON | 1 |

USB interrupt status register (R8_USB_INTR_STAT, Address R = 13h)

| Bit | Symbol | Access | Description | Reset Value |
|---|---|---|---|---|
| [7:1] | Reserved | RO | Reserved | 0000000b |
| 0 | HOST_DISCON | RO | **Host disconnect:**<br>Provides UTMI+ host port disconnect status values.<br>**0**: Connected, USB device detected on host port;<br>**1**: Disconnected, no USB device connection detected<br>Only supports high-speed USB disconnect detection, not full-speed and low-speed disconnect detection. | 0 |

USB interrupt latch register (R8_USB_INTR_L, Address R = 14h)

| Bit | Symbol | Access | Description | Reset Value |
|---|---|---|---|---|
| [7:1] | Reserved | RO | Reserved | 0000000b |
| 0 | HOST_DISCON | RO | **Host disconnect latch:**<br>Automatically set when an unmasked event occurs on HOST_DISCON. CLEARED when this register is READ | 0 |

SCARTCH register (R8_SCARTCH, Address R = 16h)

| Bit | Symbol | Access | Description | Reset Value |
|---|---|---|---|---|
| [7:0] | SCARTCH | RW | Registers used for testing, readable and writable, without affecting chip functionality | 00000000b |

USB I/O pin swap register (R8_USB_IO_SWAP, Address R = 39h/3Ah/3Bh, W = 39h, S = 3Ah, C = 3Bh)

| Bit | Symbol | Access | Description | Reset Value |
|---|---|---|---|---|
| [7:2] | Reserved | RO | Reserved | 000000b |
| 1 | USB_IO_SWAP | RW | Swap USB signal pin enable:<br>0: Do not swap D+ and D- pins;<br>1: Swap D+ and D- pins. | 0 |
| 0 | Reserved | RO | Reserved | 0 |

# Chapter 4 Parameters

## 4.1 Absolute Maximum Ratings (Critical or exceeding the absolute maximum value may cause the chip to operate improperly or even be damaged.)

| Symbol | Parameter description | Min. | Max. | Unit |
|---|---|---|---|---|
| TA | Operating ambient temperature | -40 | 85 | ℃ |
| TS | Storage ambient temperature | -55 | 150 | ℃ |
| V5 | LDO input voltage (pin V5 to power, pin GND to ground) | -0.4 | 5.5 | V |
| VDD33 | 3.3V source voltage (pin VDD33 to power, pin GND to ground) | -0.4 | 3.8 | V |
| VDDIO | ULPI interface I/O supply voltage for VDDIO pin | -0.4 | 3.8 | V |
| VUSB | Voltage on USB signal pins | -0.4 | VDD33+0.4 | V |
| VIO | Voltage on other input or output pins (excluding XI and XO) | -0.4 | VDD33+0.4<br>VDDIO+0.4 | V |
| VXI | Voltage on XI pin | -0.3 | 1.5 | V |
| VESD | HBM ESD withstand voltage on I/O pins | 6K | | V |

## 4.2 Electrical Characteristics (Test conditions: TA=25°C, V5=VDD33=3.3V, VDDIO=3.3V, no USB signal pins included)

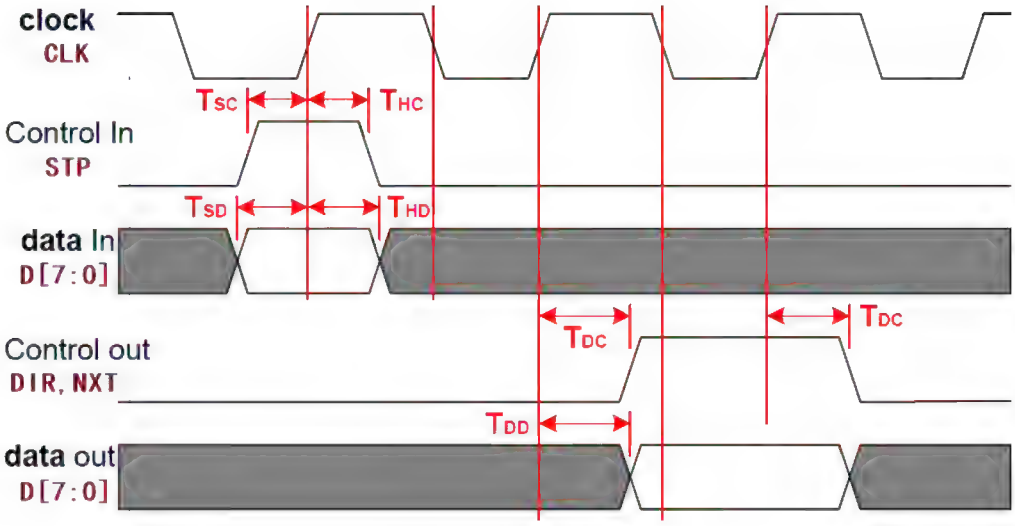
| Symbol | Parameter description | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| V5 | CH132F/B/X | LDO input supply voltage, enable internal LDO | 3.8 | 5.0 | 5.25 | V |
| | CH132A/H | | 4.5 | 5.0 | 5.25 | |
| | External input power voltage | No internal LDO required | 3.15 | 3.3 | 3.45 | |
| VDD33 | LDO output voltage | Enable internal LDO | 3.15 | 3.3 | 3.45 | V |
| | External 3.3V voltage supply | No internal LDO required | 3.15 | 3.3 | 3.45 | |
| VDDIO | ULPI interface I/O signal supply voltage | | 1.7 | 3.3 | 3.6 | V |
| ILDO | Internal power regulator LDO external load capability | | | | 30 | mA |
| ICC | Operating current during high-speed USB transfer | | | 27 | | mA |
| ICC0 | Operating current in the idle state | | | 19 | | mA |
| ISLP | Low power mode supply current (mainly internal LDO) | | | 0.13 | 0.4 | mA |
| VILXI | XI pin low level input voltage | | 0 | | 0.3 | V |

| | | | | | |
|---|---|---|---|---|---|
| VIHXI | XI pin high level input voltage | 0.9 | | 1.2 | V |
| RPD | Pull-down resistors for D7~D0 pins | 50 | 70 | 100 | KΩ |
| Vlvr | VDD33 power low voltage reset voltage threshold | 2.5 | 2.9 | 3.15 | V |
| VDDIO=3.3V | | | | | |
| VIL33 | ULPI interface I/O pin low level input voltage | 0 | | 0.8 | V |
| VIH33 | ULPI interface I/O pin high level input voltage | 1.9 | | VDDIO | V |
| VOL33 | Low level output voltage @ 8mA current input | | 0.4 | 0.6 | V |
| VOH33 | High level output voltage @ 8mA current output | VDDIO-0.6 | VDDIO-0.4 | | V |
| IPU33 | Pull-up current on the STP pin | 20 | 40 | 80 | uA |
| VDDIO=1.8V | | | | | |
| VIL18 | ULPI interface I/O pin low level input voltage | 0 | | 0.5 | V |
| VIH18 | ULPI interface I/O pin high level input voltage | 1.2 | | VDDIO | V |
| VOL18 | I/O pin low level output voltage @ input 5mA current | | 0.4 | 0.6 | V |
| VOH18 | I/O pin high level output voltage @ output 5mA current | VDDIO-0.6 | VDDIO-0.4 | | V |
| IPU18 | Low voltage reset threshold | 7 | 15 | 30 | uA |

## 4.3 Timing Parameters (Test conditions: TA=25°C, V5=VDD33=3.3V, VDDIO=3.3V)

| Symbol | Parameter description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Fxi | XI input clock frequency, XI external crystal frequency | 11.995 | 12 | 12.005 | MHz |
| Dutyxi | Duty cycle of XI input clock | 35 | 50 | 65 | % |
| Fstart | CLK clock frequency of ULPI in the initial state | 55 | 60 | 65 | MHz |
| Fsteady | CLK clock frequency of ULPI in the steady state | 59.97 | 60 | 60.03 | MHz |
| Dutycko | Duty cycle of ULPI CLK clock | 45 | 50 | 55 | % |
| Tsteady | Time from XI or CLK input clock stabilization to PLL stabilization | | 0.5 | 1.5 | mS |
| Tstart | Time from exit low-power mode to PLL stabilization | | 2 | 4 | mS |
| Trpor | Time from power on or low voltage reset to normal operation | 10 | 14 | 17 | mS |
| Twreset | RESET# pin input reset low level pulse width | 2 | | | uS |
| | RESET pin input reset high level pulse width | 2 | | | uS |
| Trreset | Pin input reset to normal operation time | 10 | 13 | 15 | mS |
| Output ULPI clock mode | | | | | |

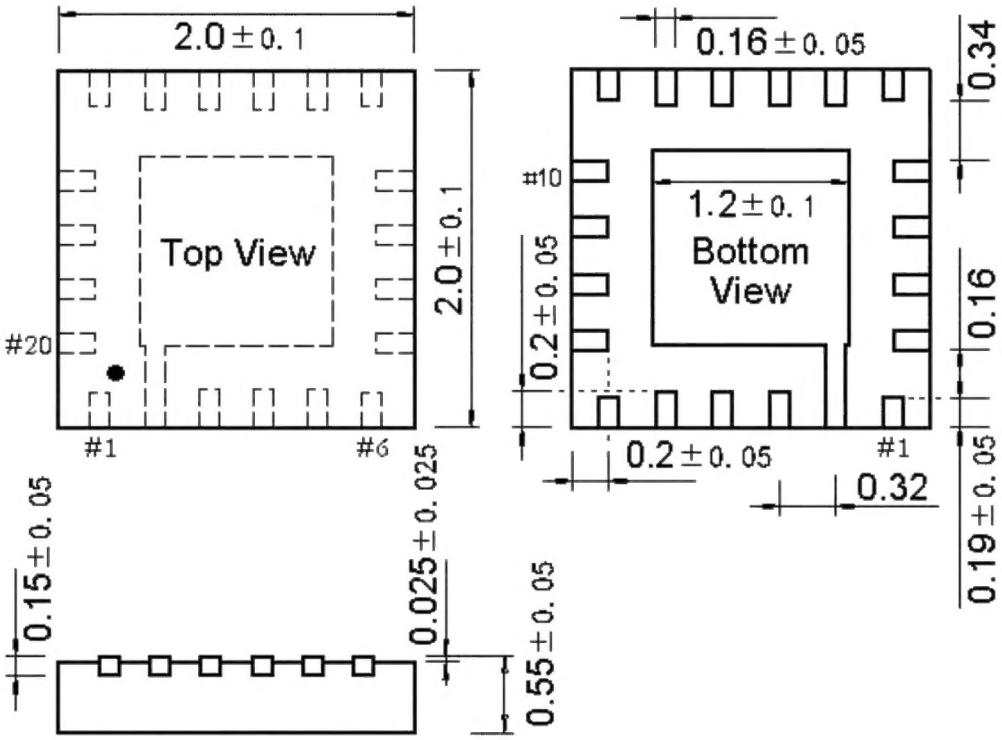
| | | | | | |
|---|---|---|---|---|---|
| TSC | STP input setup time | | | 6 | nS |
| THC | STP input hold time | 0 | | | nS |
| TSD | Data D0~D7 input setup time | | | 6 | nS |
| THD | Data D0～D7 input hold time | 0 | | | nS |
| TDC | Valid delay time for DIR or NXT output | 0.8 | | 6 | nS |
| TDD | Valid delay time for Data D0~D7 output | 0.8 | | 8 | nS |
| Input ULPI clock mode | | | | | |
| TSC | STP input setup time | | | 2.5 | nS |
| THC | STP input hold time | 1 | | | nS |
| TSD | Data D0~D7 input setup time | | | 2.5 | nS |
| THD | Data D0～D7 input hold time | 1 | | | nS |
| TDC | Valid delay time for DIR or NXT output | 1.5 | | 6.5 | nS |
| TDD | Valid delay time for Data D0~D7 output | 1.5 | | 7 | nS |



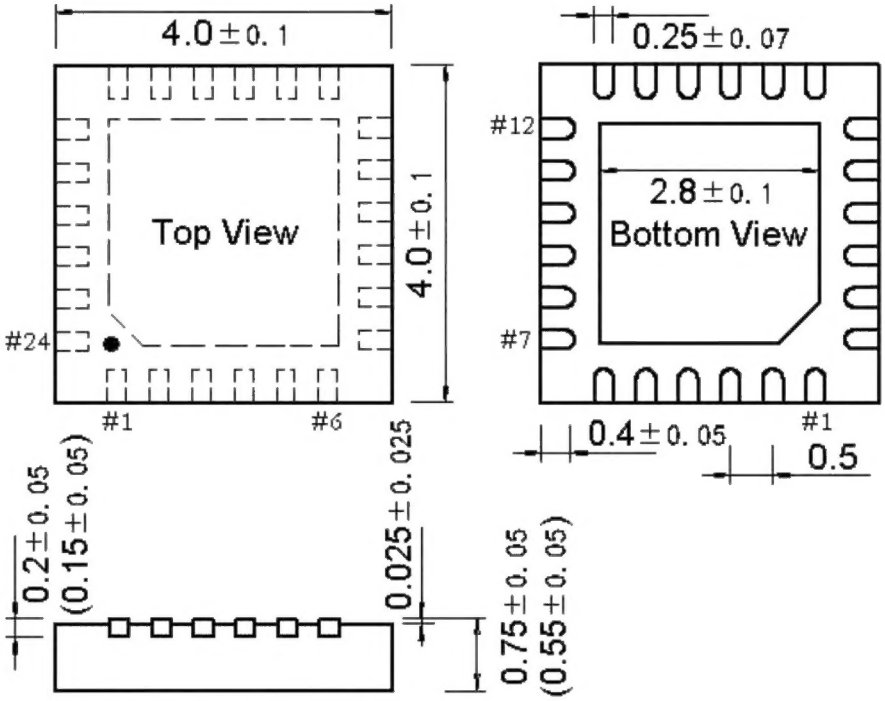
# Chapter 5 Package Information

*Note:*
*All dimensions are in millimeters.*
*The pin center spacing values are nominal, without error. And the error of dimensions other than the pin center spacing values is not more than ±0.2mm.*

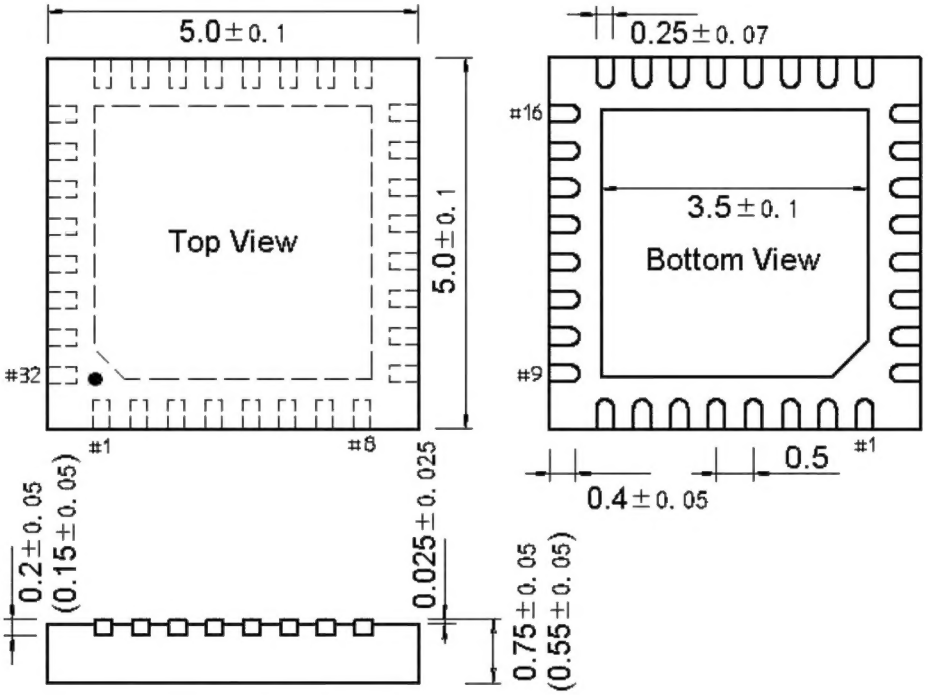
## 5.1 QFN20C_2x2




## 5.2 QFN24_4x4



## 5.3 QFN32_5x5


5.0±0.1
Top View
5.0±0.1
#32
#1
#8
0.25±0.07
#16
3.5±0.1
Bottom View
#9
#1
0.5
0.4±0.05
0.2±0.05
(0.15±0.05)
0.025±0.025
0.75±0.05
(0.55±0.05)

# Chapter 6 Applications

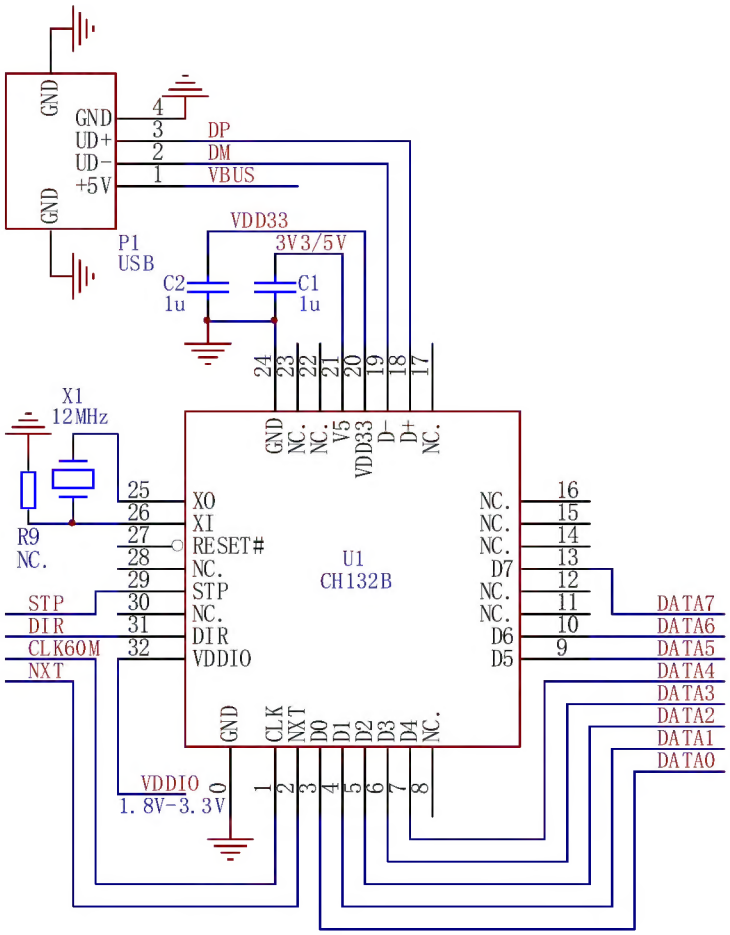
## 6.1 Minimum System

The CH132 acts as a USB PHY for the microcontroller and requires 12 signal lines to be connected. The crystal in the diagram can be replaced by the 12MHz clock provided by the microcontroller or FPGA (Note that the XI pin voltage is only 1.2V, or change to CLK clock input mode). The RESET# pin is an optional connection and is left dangling by default. The C1 and C2 capacitors (MLCC) are optional in the 1uF~4.7uF range.

VDDIO is the power supply of ULPI interface I/O pins, need to add 0.1uF~1uF decoupling capacitor, VDDIO voltage should be the same as the I/O voltage of MCU or FPGA.

It is recommended that the CH132 be externally powered with a preferred 3.3V input from both V5 and VDD33.

In the figure, R9 is not connected by default, it is the ULPI clock output mode, and the CLK pin outputs a 60MHz clock. If R9 is short-circuited, the input ULPI clock mode is enabled, X1 can be removed, and the external 60MHz clock is input from the CLK pin.




## 6.2 HOST Application with VBUS Power Control

CH132 is used as a USB PHY for MCU or FPGA, 12 signal lines need to be connected. RESET# pin is an optional connection, default is dangling, if connected, it is recommended that the other driver is set to open-drain output. The XI and XO pins of the CH132 have built-in crystal oscillator capacitors, and the external one only needs crystal X1.If the MCU or FPGA can provide a 12MHz clock then You can remove

crystal X1 and change R3 to 0 (Note that the XI pin voltage is only 1.2V, or change to CLK clock input mode).MLCC capacitor C2 can be selected from 1uF to 10uF, and it is recommended to connect another 0.1uF in parallel.

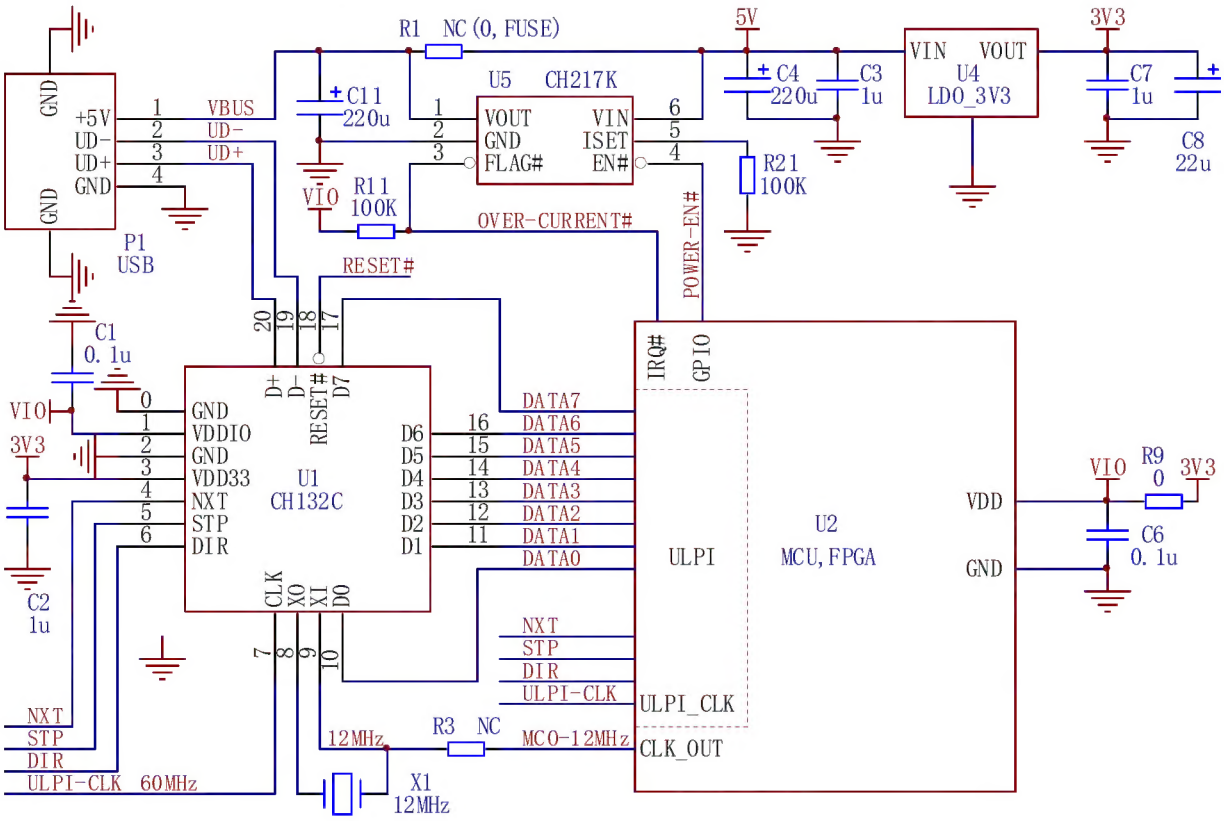
The small CH132C is preferred in the figure, with both VDD33 and V5 using the same externally supplied 3.3V power supply as the MCU or FPGA.

For USB host applications that also require 5V power to VBUS, it is recommended to consider VBUS overcurrent protection, refer to the diagram below for optional CH217 or similar USB current-limiting power switch chip and control by MCU or FPGA to implement VBUS overcurrent protection. If the internal LDO of CH132 is enabled, it is recommended to replace C2 with two capacitors of 0.1uF and 10uF in parallel to avoid the 5V reduction affecting VDD33 and thus causing CH132 reset. In the figure, the internal LDO is not enabled in CH132.

Simple USB host application can also use 300mA~1A fuse resistor R1 instead of U5, R11, R21 in the figure.

For USB device applications, you can get 5V power from VBUS, refer to the following diagram to remove U5, R11, R21 and C11, and change R1 to 0 or insurance resistor, C4 is reduced to within 10uF according to USB specification. The three power supply schemes are as follows:

①Self-powered 3.3V scheme, without VBUS power, if you need to detect can also be VBUS through the 10KΩ resistor into the MCU pins for detection;

②External LDO step-down scheme, through the external LDO VBUS down to 3.3V for MCU and CH132 use, refer to the following figure U4 step-down;

③Internal LDO step-down scheme, if the MCU power consumption is small, then it can also be unified by the CH132 internal LDO step-down power supply 3.3V, but C2 needs to be increased appropriately, and VBUS needs to add overvoltage protection devices.